AMENDMENTS TO THE CLAIMS

In the Claims

Please amend the claims as follows:

Claim 1. (Previously Amended): A circuit protected against transient disturbances, the circuit comprising:

a combinatory logic circuit having at least one output:

a means for generating an error control code for said at least one output; and

a memory element coupled to said means for generating an error control code and coupled to said combinatory logic circuit so as to receive the at least one output and the error control code, the memory element being controlled by the means for generating an error control code to be transparent when the error control code indicates that no transient disturbance has occurred, and to keep the state of said at least one output unchanged when the error control code indicates that a transient disturbance has occurred.

Claim 2. (Previously Amended): The protected circuit of claim 1, wherein the means for generating an error control code comprises a circuit for calculating a parity bit for said output and a circuit for checking the parity of the output and of the parity bit.

Claim 3. (Previously Amended): The protected circuit of claim 1, wherein the means for generating an error control code comprises a duplicated combinatory logic circuit, said memory element being provided to be transparent when the outputs of the logic circuit and of the duplicated circuit are identical, and to keep its state when said outputs are different.

Claim 4. (Previously Amended): The protected circuit of claim 1, wherein the means for generating an error control code includes an element for delaying said at

least one output by a predetermined duration greater than the maximum duration of transient errors, said memory element being provided to be transparent when outputs of the logic circuit and of the delay element are identical, and to keep its state when said outputs are different.

Claim 5. (Previously Amended): The protected circuit of claim 3, wherein said memory element is formed from a logic gate providing said output of the logic circuit, this logic gate including at least two first transistors controlled by a signal of the logic circuit and at least two second transistors controlled by a corresponding signal of the duplicated circuit, each of the second transistors being connected in series with a respective one of the first transistors.

Claim 6. (Currently Amended): A circuit protected against transient disturbances, the circuit comprising:

a combinatory logic circuit having at least one output, said at least one output having a value at an occurrence of a clock edge and maintaining this value at least for a determined time period in the absence of disturbances;

a first flip-flop connected to said at least one output and rated by a clock~~, the first flip-flop being connected to receive said output~~;

a second flip-flop connected to said at least one output and rated by the clock delayed by a predetermined ~~duration~~ delay shorter than said time period; and

a circuit for analyzing outputs of the flip-flops, the analysis circuit indicating an error if the flip-flop outputs are different.

Claim 7. (Previously Amended): The protected circuit of claim 6, wherein the second flip-flop is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

Claim 8. (Previously Cancelled).

Claim 9. (Previously Amended): A circuit protected against transient disturbances, the circuit comprising:

three identical logic circuits, wherein each of the logic circuits is preceded by a two-input memory element respectively receiving outputs of the two other logic circuits as the memory element's inputs, each memory element being provided to be transparent when its two inputs are identical, and to keep its state unchanged when the two inputs are different.

Claim 10. (Previously Amended): The protected circuit of claim 9, wherein the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and a second input of the memory element being connected to the gates of the two other transistors.

Claim 11. (Previously Cancelled).

Claim 12. (Previously added). A circuit protected against transient disturbances comprising:

a combinatory logic circuit having at least one output;

a circuit for generating an error control code for said at least one output, said circuit for generating an error control code selected from a group of circuits consisting of a parity generation circuit and a circuit that is a duplicate of the combinatory logic circuit; and

a memory element coupled to said circuit for generating an error control code and to said combinatory logic circuit, the memory element being controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect;

wherein said control code is correct when a parity generation circuit is used and when the output from the parity generation circuit is inactive, said control code being incorrect when the output from the parity generation circuit is active, and wherein

said control code is correct when a duplicate of the combinatory logic circuit is used and when the output from the duplicate of the combinatory logic circuit is identical to the output of the combinatory logic circuit, said control code being incorrect when the output from the duplicate of the combinatory logic circuit is not identical to the output of the combinatory logic circuit.